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Loss Model for Gallium Nitride DC-DC Buck Converter

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***Abstract*—In recent years, more research has been done on Enhancement Mode Gallium Nitride (eGaN) converters as the world is moving towards more power efficient converters. The process to make converters more efficient was complicated and slow in the twentieth century. With help of simulation tools such as MATLAB and LTspice, this process has become much faster and reliable in the modern era. In order to make this process even faster, one of the important aspects in power electronics is to evaluate different losses in the converter. A model for estimating power losses for eGaN DC-DC buck converter (12V/1.2V) is illustrated in this paper. This loss model was calculated for different frequencies and compared experimentally and theoretically. This paper also investigated the constant variables which help realize the difference between theoretical and experimental losses in eGaN DC-DC buck converter.**

I. Introduction

As eGaN power transistors appear to be most promising candidates to replace silicon power Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs), eGaN power converters could also be promising candidates to replace silicon based power converters [1]. There has been a tremendous amount of research done on losses specific to eGaN power transistors, such as switching losses, but very little research has been done on the losses of the eGaN converter as whole. One of the organization that is leading this campaign is Efficient Power Conversion (EPC) which was founded in 2007. According to EPC, power based converters not only improve the efficiency of electrical power but also enable new, life-changing applications that did not exist five years ago [2]. This research also used EPC 9036 eGaN half bridge DC-DC synchronous buck converter development board as shown in Figure 1 to study the loss model. Buck converter was chosen because of its simplicity and wide use in the power electronics world for testing purposes. The loss model referred to total loss in the buck converter.

The proposed loss model included eGaN power transistor losses, inductor loss, and capacitor loss. The eGaN power transistor losses included conduction loss on high side and low side, switching loss on high side, and gate driver loss. Switching loss on low side was very small thus neglected. Other losses, such as dead time loss and output capacitance loss, were also included. A synchronous buck converter consisted of two power transistors which helped improve efficiency by neglecting diode loss. Choosing a right inductor and a capacitor to improve loss model was one of the important task as development board provided flexibility to design your own filter.

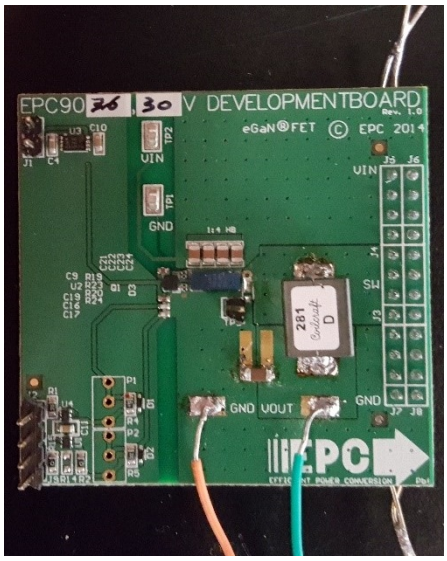

Fig. 1: eGaN DC-DC buck converter

The power electronics industry projected that by 2025, 80% of the time will be spent working on the modeling and simulating and only 20% on hardware prototyping [3]. This method will decrease the amount of iterative hardware prototyping require before successfully achieving goals. One of the aspects of this research was to evaluate the constant variables in the different losses which help realize the difference between experimental and theoretical loss models. The next hardware prototyping of this converter will be much more efficient and reduce the iterative process when keeping in mind these constant variables.

II. Methodology

Three different methods were used to validate the results and to make appropriate conclusion: A. Experimental Analysis, B. Theoretical Analysis, C. LTspice Simulation.

A. Experimental Analysis

For this experiment, the first challenge faced was to choose the right inductor and capacitor. The best method was to use the simulation tool LTspice, which shows the stability of the buck converter when different combination of inductor and capacitor values are chosen. The stability of the system was excellent when the combination of 280nH inductor and 10uF capacitor were used in the LTspice simulation. During the experiment, initial input voltage was set to 0V and slowly increased to its final value of 12V to further ensure the stability of the system. Further discussion on this is in the LTspice simulation section.

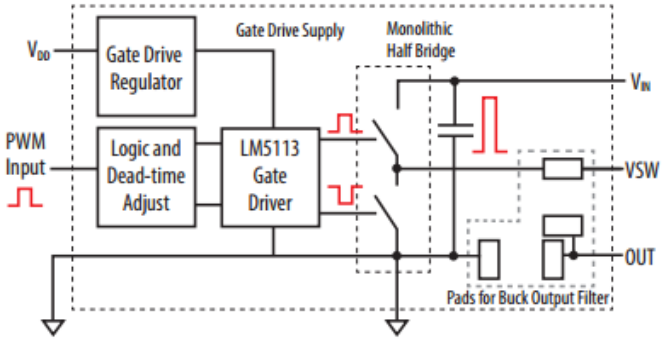

Fig. 2: eGaN DC-DC buck converter block diagram [4]

A block diagram for the development board is shown in Figure 2 to understand the eGaN buck converter development board. The input voltage (Vin) was 12V DC power supply connected straight to HS eGaN transistor. The gate drive voltage (VDD) provided between 7-12V DC power to turn on the eGaN transistor which produced a flow of current in the drain. The pulse width modulation (PWM) input provided the duty ratio of 10%, amplitude 3V peak to peak, and 1MHz or 500kHz frequency to step down the voltage to 1.2V, and assisted in switching HS and LS eGaN transistors.

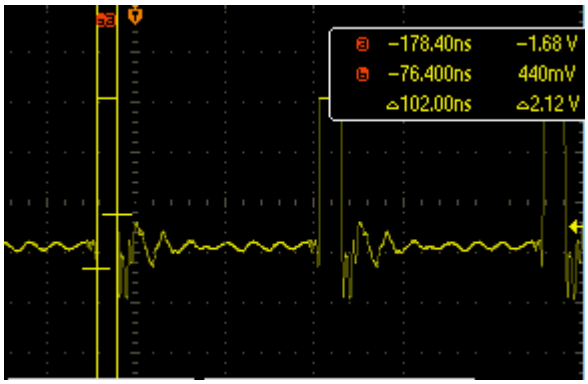

Fig. 3: Switch node measurement at 1MHz on oscilloscope

For this particular experiment, the data gathered at 500kHz and 1MHz in order to analyze the data accurately and provide an unbiased conclusion. On the development board, the switch node terminal and ground terminal were specifically designed to observe the switching frequency in the oscilloscope. Figure 3 and 4 provide confirmation of the duty ratio of PWM at 1MHz and 500kHz respectively.

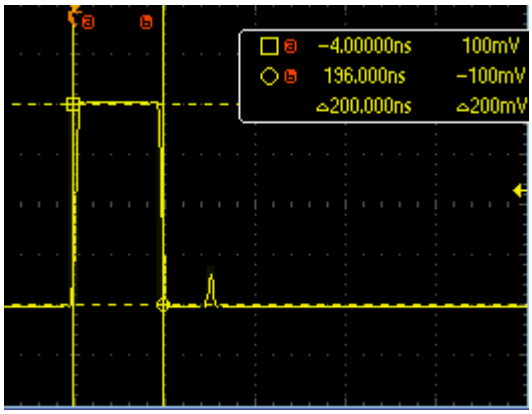

Fig. 4: Switch node measurement at 500kHz on oscilloscope

To obtain a various range of output current, an electric load was considered. The electric load set the constant output current as desired and made any changes as needed. To ensure the quality measurement and avoid any resistance in the wire, kelvin (4-wire) resistance measurement method was used. The input current and input voltage was directly measured from the development board. The electric load also had voltage-sensing capabilities which accurately provided output voltage at the load. The duty ratio of PWM had to be increased slightly at higher output currents as the input current of the power supply was limited to maximum of 3.3 A. The efficiency was calculated from experimental input power and output power.

B. Theoretical Analysis

In order to evaluate different losses in the EPC 9036 development board, previous loss model datasheet from fair-child was used as a reference [5]. The datasheet provided a basic idea of different losses in the synchronous buck converter.Because the loss model needed to be as explicit as possible, considering other datasheets would improve the loss model and make it as accurate as possible. Loss model datasheet from Texas Instrument provided precise equations to study in depth the different losses in the buck converter [6-7].

Power losses in the synchronous buck converter included several parts: eGaN transistors loss, inductor loss, capacitor loss etc. Among these, eGaN transistor loss contributed a significant part of the loss model. The first loss associated with eGaN transistor was conduction loss. The on resistance on the eGaN transistor and the RMS current determined conduction loss. Specifically, the conduction losses were divided into high side (HS) eGaN transistor loss and low side (LS) eGaN transistor loss as shown in equation (1) and (2).

The RMS current used in equation (1) and (2) was calculated by equation (3) and (4) for HS and LS eGaN transistor respectively. The ripple current is given by equation (5).

$$P_{cond(HS)} = R_{ds(ON)HS} * I^2_{RMS(HS)} \tag{1}$$

$$P_{cond(LS)} = R_{ds(ON)LS} * I^2_{RMS(LS)} \tag{2}$$

$$I_{RMS(HS)} = \sqrt{\frac{D}{3} * \left((I_{out} + \frac{I_{ripple}}{2})^2 (I_{out} \right.}$$

$$\left. \sqrt{+\frac{I_{ripple}}{2}) * (I_{out} - \frac{I_{ripple}}{2}) + (I_{out} - \frac{I_{ripple}}{2})^2} \right) \tag{3}$$

$$I_{RMS(LS)} = \sqrt{\frac{1-D}{3} * \left((I_{out} + \frac{I_{ripple}}{2})^2 (I_{out} \right.}$$

$$\left. \sqrt{+\frac{I_{ripple}}{2}) * (I_{out} - \frac{I_{ripple}}{2}) + (I_{out} - \frac{I_{ripple}}{2})^2} \right) \tag{4}$$

$$I_{ripple} = \frac{(V_{in} - V_{out}) * D * Tsw}{L} \tag{5}$$

The second loss associated with eGaN transistor was switching loss. Switching loss was composed of HS and LS switching loss in eGaN transistor, gate drive loss, deadtime loss and output capacitance loss. Switching loss on HS was induced during turn on and turn off transition due to the LS clamping effects, which causes HS affected by both high current and high voltage at the same time. HS switching loss and HS gate current is given by equation (6) and equation (7) respectively. Considering LS eGaN transistor, both LS turnon and turnoff were soft switching at normal operations. Therefore, the LS switching loss was small and thus neglected in this report.

$$P_{sw(HS)} = V_{in} * I_{out} * f_{sw} * \frac{Q_{sw}}{I_g} \tag{6}$$

$$I_g = \frac{V_{Driver} - V_{PL}}{R_g + R_{Driver}} \tag{7}$$

Deadtime loss was induced by LS eGaN transistor during dead-times and can be calculated by equation (8). The gate drive loss is given by equation (9). The deadtime during rise and fall is given by equations (10) and (11).

$$P_{deadtime} = V_{SD} * \left((I_{out} - \frac{I_{ripple}}{2}) * t_{deadtime(rise)} \right.$$

$$\left. +(I_{out} + \frac{I_{ripple}}{2}) * t_{deadtime(fall)} \right) * f_{sw} \tag{8}$$

$$P_{gate} = P_{gate(HS)} + P_{gate(LS)}$$

$$P_{gate} = (Q_{g(HS)} + Q_{g(LS)}) * V_{Driver} * f_{sw} \tag{9}$$

$$t_{deadtime(rise)} \approx t_{delay(rise)} \tag{10}$$

$$t_{deadtime(fall)} = t_{delay(fall)} + \frac{Q_{gs(LS} * (R_{gate} + R_{driver})}{V_{driver} - \frac{V_{th}}{2}} \tag{11}$$

Another eGaN transistor related power loss in synchronous buck converters was eGaN output capacitance loss, which was induced by output capacitance charge/discharge. The output capacitance loss for HS and LS is given by equation (12) and (13) respectively.

$$P_{Coss(HS)} = 0.5 * Q_{oss(HS)} * V^2_{in} * f_{sw} \tag{12}$$

$$P_{Coss(LS)} = 0.5 * Q_{oss(LS)} * V^2_{in} * f_{sw} \tag{13}$$

DC Resistance (DCR) in inductor and Equivalent Series Resistance (ESR) in capacitor were directly proportional to the inductor and capacitor loss. The 280nH inductor and 10uF capacitor used in the development board had very low DCR and ESR values, which minimized the inductor loss and capacitor loss. Inductor loss and capacitor loss are provided by equation (14) and equation (15) respectively. The RMS current on the inductor was calculated by equation (16).

$$P_{DCL} = I^2_{RMS(L)} * DCR \tag{14}$$

$$P_{DCC} = I^2_{ripple} * ESR \tag{15}$$

$$I_{RMS(L)} = \sqrt{I^2_{out} + \frac{I^2_{ripple}}{12}} \tag{16}$$

The datasheet of the eGaN transistor EPC 2100 provided all of the values for the parameters as most of those losses are associated with transistor loss [8]. Datasheets for inductor and capacitor are obtained from Coilcraft and Digikey respectively [9-10]. Table I provides all the values for the parameters in equation (1) to (16).

TABLE I. PARAMETER AND ITS VALUE

Parameter	Value
V_{in}	$12V$
V_{out}	$1.2V$
L	$280nH$
C	$10uF$
f_{sw}	$1MHz/500kHz$
T_{sw}	$1\mu s/2\mu s$
I_{out}	$0A$ *to* $32A$
$R_{ds(ON)HS}$	$6m\Omega$
$R_{ds(ON)LS}$	$1.5m\Omega$
V_{driver}	$10V$
R_{gate}	0.3Ω
R_{driver}	2.7Ω
$Q_{sw(HS)}$	$1.1nC$
$Q_{g(HS)}$	$3.5nC$
$Q_{g(LS)}$	$15nC$
$t_{delay(rise)}$	$650ns$
$t_{delay(fall)}$	$750ns$
$Q_{gs(LS)}$	$4.6nC$
V_{th}	$2V$
V_{sd}	$1.8V$
$C_{oss(HS)}$	$290pF$
$C_{oss(LS)}$	$1600epF$
DCR	$.29m\Omega$
ESR	$1.5m\Omega$

All individual losses were added together to calculate total loss in the eGaN buck converter. The output power was easily obtained as the output current and output voltage were known parameters. The total loss was added to output power to get input power. Finally, efficiency was obtained when output power was divided by input power.

Because of the wide range of the output current from 0 to 32 amps, it was more complicated and more time consuming if it was done by hand. In order to reduce the complexity, a programming tool name MATLAB was used which made the calculation easy and less time consuming. MATLAB has a unique feature that allowed a variable to define in a range. With the help of this feature, output current was defined from 0 to 32 amps with increment of 0.032 to ensure precise curve of efficiency. The efficiency versus output current graph was plotted at 500kHz and 1MHz in order to make the accurate conclusion.

C. LTspice Simulation

One of the advantages of using LTspice Simulation was that it provided more option to check your results and to ensure that progress was made in the right direction. As mentioned earlier, LTspice simulation initially used to figure out the right inductor and capacitor for the development board. The stability of the system was sufficient to confirm that 280nH inductor and 10uF capacitor would work experimentally.

The LTspice model of the development board is shown in the Figure 5. To justify results from LTspice, losses such as inductor loss, capacitor loss, gate drive loss, etc. are also modeled as shown in Figure 5. The LTspice model for the inductor and its parameters are provided on Coilcraft's

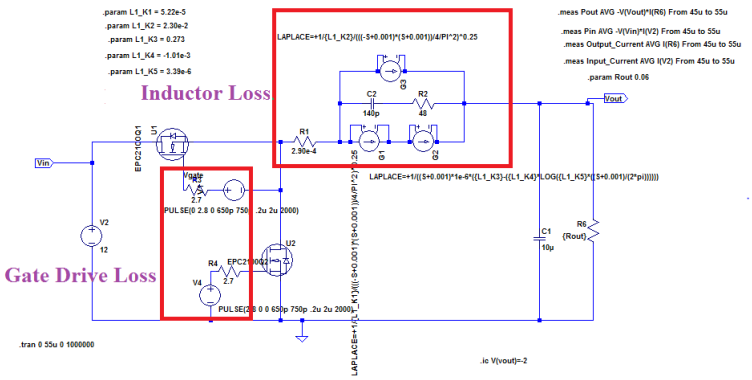

Fig. 5: Pspice model for development board

website [11]. The gate drive loss modeled with a resistor in series with the gate and the PWM source. The LTspice model used for EPC2100 eGaN transistor provided on EPC's website [12]. Therefore, all the transistor related losses are embedded inside the EPC2100 eGaN transistor model. The capacitor loss is also embedded inside the capacitor model in the LTspice.

Spice directives that measured the input current, input voltage, output current and, ouput voltage in the LTspice were used to receive precise measurements. Changing the load resistance provided a various range of output current as well as adding initial condition produce faster simulation. The initial condition was changed depending upon the output current. The LTspice simulation was also done at 500kHz and 1MHz frequency.

III. Results and Discussion

The theoretical efficiency was collected for two different frequencies with the help of MATLAB. Because the output current included one thousand points (increment of 0.032 from 0 to 32), it was impossible to contain all the results in this paper. Therefore, those points were plotted in a graph to make comparison with experimental efficiency and efficiency from LTspice simulation at 1MHz as shown in Figure 6.

Looking at similarities of the theoretical and experimental efficiency, both have a similar kind of trend. However, comparing both there were huge differences. At lower current, the experimental efficiency had higher efficiency than theoretical efficiency. Once output current reached 6 A, the theoretical efficiency was higher than experimental efficiency. The purpose of plotting LTspice efficiency was accomplished as it clearly matches with experimental efficiency. The similar kind of characteristics can also seen at 500kHz in Figure 7.

From these plots, two loss models showing the loss difference between theoretical and experimental were plotted at 1MHz and 500kHz as shown in Figure 8 and 9 respectively. Both of these plots show similar trends. In fact, the loss difference approaches 0 watts approximately at 10 A in

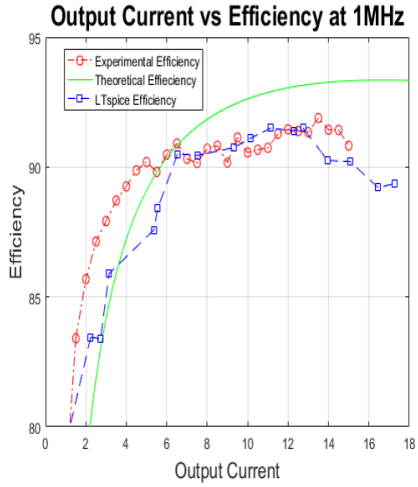

Fig. 6: Output current vs efficiency plot at 1MHz

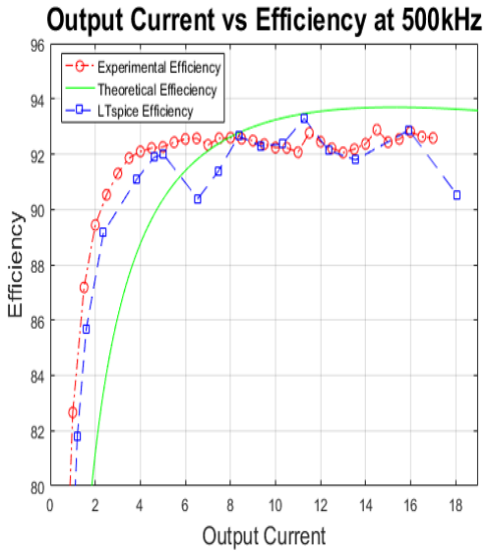

Fig. 7: Output current vs efficiency plot at 500kHz

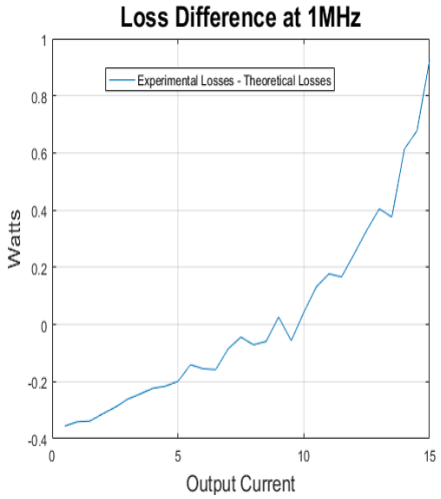

Fig. 8: Loss difference at 1MHz

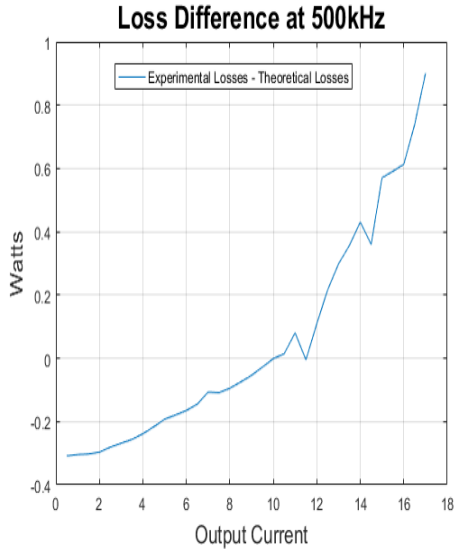

Fig. 9: Loss difference at 500kHz

both cases. However, this does not prove that frequency is independent to obtain an accurate loss model.

In order to point out the exact variables that contributed in the loss difference, curve fitting tool from MATLAB was used to check the error. Figures 10 and 11 show that second order polynomial method fits the best through all the points. This indicated that any equation with second order polynomial may have caused the loss difference.

Equations (1),(2),(14), and (15) are the ones with second order equation. From these equations, following variables were tested experimentally to verify the loss model: Rdson HS, Rdson LS, ESR, and DCR. The Rdson on HS was measured between 5mΩ and 7mΩ, while Rdson on LS was measured between 1mΩ and 2.2mΩ. The theoretical values for HS and LS are 6mΩ and 1.5mΩ. Therefore, Rdson on HS and LS do not contribute to the loss difference. When DCR of the inductor was measured, the experimental value was between

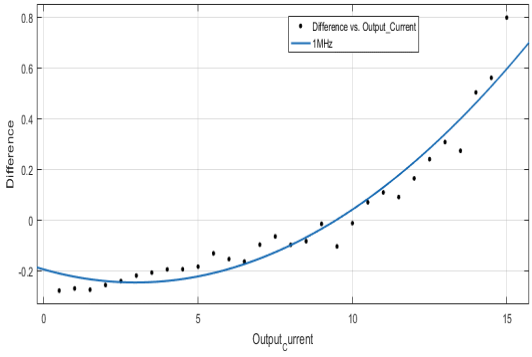

Fig. 10: Second order polynomial loss difference at 1MHz

1mΩ and 3mΩ. This range of values were much higher than theoretical value of .29Ω. This clearly indicated that DCR did make contribution in loss difference. To confirm

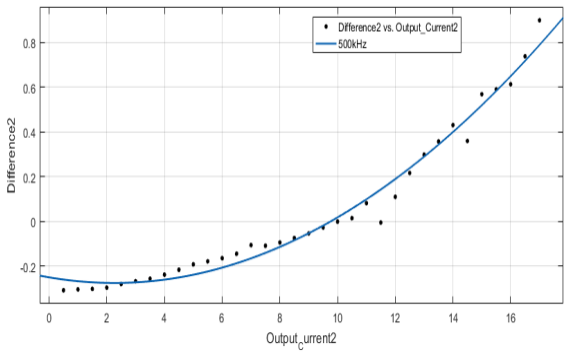

Fig. 11: Second order polynomial loss difference at 500kHz

further, the theoretical value was changed from .29mΩ to 2mΩ. The new plot shown in Figure 12 and 13 clearly suggested that ESR was one of the variable as the theoretical and experimental efficiency matched closely after 6A of output current. The method attempted to measure the ESR on the capacitor experimentally was not precise enough to conclude that ESR was also part of the loss difference.

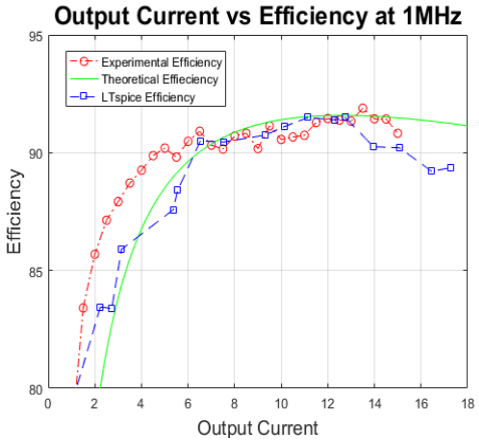

Fig. 12: After changing theoretical value from .29mΩ to 2mΩ at 1MHz

IV. Conclusion and Future Work

The power converters will keep evolving to improve efficiency as the technology that uses will evolve. Having a known loss model for a converter is very useful to improve efficiency in less time and less iterative process for hardware prototyping. This research showed that the loss difference between experimental and theoretical data was caused by DCR of an inductor. Although DCR is one of such variables that are at the fault. In the future, more detailed experiments can be done to test different variables.. Measurements that are more precise will also help to make the loss model as accurate as possible. Some known facts such as the initial difference between experimental and theoretical efficiency can also be resolved in the future. New designs with different capacitors and inductors to produce new loss model and compare with

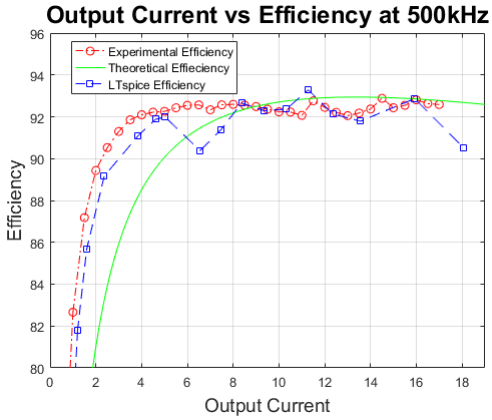

Fig. 13: After changing theoretical value from .29mΩ to 2mΩ at 500kHz

current loss model can also be useful to know the behavior of it.

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