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# UTILIZING STANDARD CMOS PROCESS FLOATING GATE DEVICES FOR ANALOG DESIGN

By

Jacob Killens

A Thesis
Submitted to the Faculty of
Mississippi State University
in Partial Fulfillment of the Requirements
for the Degree of Master of Science
in Electrical Engineering
in the Department of Electrical and Computer Engineering

Mississippi State, Mississippi

August 2001

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Jacob Killens

2001

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This thesis examines a floating gate device (FGD) structure available under standard (digital) CMOS manufacturing processes and puts forth two applications for these devices.

The first application is the creation of a tunable current mirror. Inclusion of the FGD structure allows the legs of the mirror to be electronically tweaked to compensate for mismatch. Experimental data is presented on this device structure's performance.

The second application explores using the FGD structure as a tunable resistor. Operation of the FGD in this manner creates the possibility of an electrically tunable beta-multiplier current reference. This tunability allows theoretical adjustment of both the generated reference current as well as a selectable temperature performance. Experimental data of obtained resistor values is presented with simulation results of the entire circuit.

# ACKNOWLEDGMENTS

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# CHAPTER I

# INTRODUCTION

Although integrated circuit processing is the most precise manufacturing technique in history, it is still not perfect. Oxide encroachment and other forms of process variation combine to make the task of having a given circuit perform exactly as expected extremely challenging. Other environmental effects, such as temperature variation, may also cause performance deviance.

Design techniques such as common-centroid layout and using device sizes much larger than process minimums can help to reduce the manufacturing induced error in systems, but these practices are far from perfect.

A more reliable alternative is to design circuits so that critical components can be adjusted after fabrication to compensate for both manufacturing problems as well as a given operating environment. Traditionally this has required laser trimming or non-standard manufacturing steps for special structures; these techniques tend to be slow, limited in scope, or expensive.

This thesis explores the use of an innovative programmable device structure that is available in standard CMOS processes to allow post manufacturing electric tunability to critical design areas. Two commonly used circuits that are typically sensitive analog designs are examined to see how much benefit including such tunability will provide.

This thesis begins by examining a floating gate device (FGD) that will allow design tunability when properly utilized. The FGD's operating characteristics and adjustability will be examined. Next, the FGD will be used to modify a simple current mirror. This modification will be tested for its ability to tune out mismatch and produce well matched currents. Finally, a tunable current reference will be put forth. This circuit's ability to handle fine tuning adjustments to its current output as well as its temperature characteristics will be discussed. Possible future works concerning FGDs shall be put forth at the end of the thesis.

# CHAPTER II

# PROGRAMMABLE STRUCTURE

## 2.1 Overview

The device providing an electrical tunability for the two circuits presented is Ohsaki's EEPROM floating gate device (FGD) structure for standard CMOS processes [1]. This innovative design allows a tunable threshold MOSFET to be implemented in a single polysilicon layer process without additional fabrication steps (beyond the standard CMOS process flow).

## 2.2 Physical Structure of Programmable Device

The device structure consists of two MOSFETs, one *p*MOS and one *n*MOS, connected together through the joining of their gates as shown in Figure 2.1.

As one would expect with the FGD structure being designed to operate as a MOSFET, the external connections of the device strongly resemble conventional MOSFET nodes. The source and drain connections are created exactly as they are in a normal MOSFET using the appropriate half of the FGD structure as shown in Figure 2.1.

The device type is determined by how the external leads are connected since this type of FGD contains both FET types. The particular configuration shown in Figure 2.1 creates the *n*MOS version of the Ohsaki structure by connecting the *n*+ regions of the

*n*MOS structure as the source and drain connections for the device. Utilizing technologies that provide isolation of the bulk on the *n*MOS side of the FGD, such as Silicon-on-Insulator (SOI), creates the possibility of a *p*MOS flavor of the FGD by allowing more control gate drive than simply driving the source and drain. Notice that the joined gates have no external connections. This forms the floating gate of the FGD structure.

The gate connection, however, does differ from the conventional form. The gate connection (or "control gate") is formed by taking all of the connections of the device that are on the opposite half of the FGD (the source, drain, and body connections) and tying them together (such as in a MOSCAP). This connection is labeled "control gate" in Figure 2.1 and is formed from the *p*MOS section of the FGD.

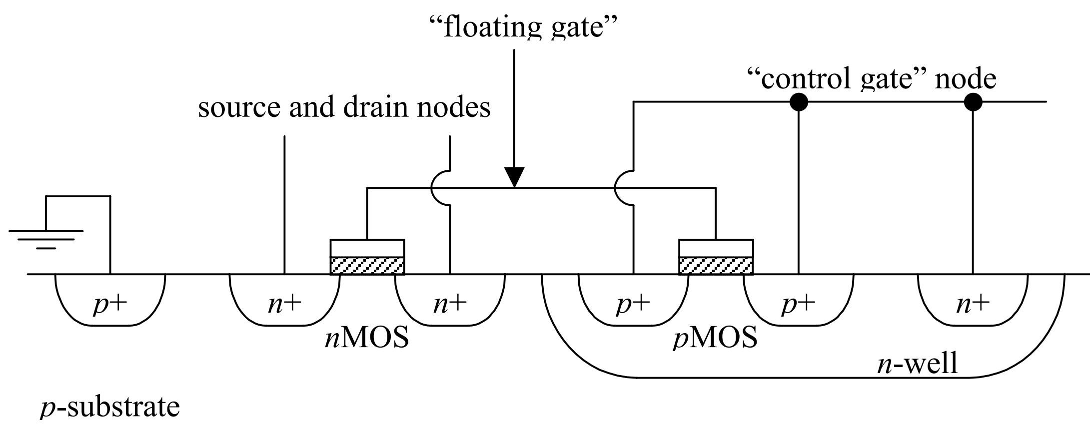


Figure 2.1. Single-poly FGD Structure [2]

## 2.3 Operating Characteristics of Programmable Structures

Under normal circumstances this programmable structure operates exactly as a conventional MOSFET of the appropriate type (*n*MOS or *p*MOS). Each of the external connections (source, drain, and control gate) function as they would for any other MOSFET. What makes this structure different is the inclusion of an internal floating gate.

The floating gate is used as a charge storing area. By varying the amount of charge trapped on this gate, the operator can vary the threshold voltage of the MOS device, effectively creating a voltage level shift. The trapped charge creates a virtual voltage source that functions like that shown in Figure 2.2 where $V_{ADJ}$ is the DC voltage adjustment to the MOS threshold voltage induced by charge trapped on the floating gate. Simulations attempting simple modification of model parameters, such as using the common radiation induced threshold shift-modeling technique of adjusting VTO [3] produced results that conflicted with experimentation. Depending upon the amount of charge trapped, this shifting allows a variation of the threshold over a positive or negative range. Thus, a single FGD structure can function as an enhancement-mode MOSFET or as a depletion-mode MOSFET. This charge storing technique is very popular with a wide variety of conventional programmable devices. The difference is that historical use of this principle has required a second layer of polysilicon to be formed as the external control gate [4]. Many EEPROM structures described as standard process devices, while

not requiring a second polysilicon layer, do require add-ons such as current injection ports as in [5]. The Ohsaki FGD is unique in that it does not require two polysilicon layers or any other specialized processing.

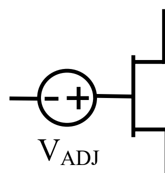


Figure 2.2. Model of Floating Gate Threshold Voltage Adjustment

## 2.4 Programming/Deprogramming Techniques

This thesis defines programming a FGD as increasing the number of electrons trapped on the floating gate of the device, which increases the *n*MOS threshold voltage, $V_{TH}$. Deprogramming, or erasing, is the exact opposite operation.

There are two methods of performing both of these procedures. The first method, Fowler-Nordheim tunneling, is both the most flexible and most predictable method. Fowler-Nordheim tunneling is accomplished by creating a powerful field across a gate oxide that enables electrons to tunnel through the oxide. The two key guidelines to this type of programming and deprogramming are insuring the field strength is high enough to enable tunneling (6.4 MV/cm [6]), while maintaining low enough field strength to prevent oxide destruction. Following these criteria result in a tunneling current density described by [4]

$$J\left[\frac{A}{m^2}\right] = 1.15\cdot 10^{-6} \cdot E_{inj}^2 \cdot e^{\left[\frac{-2.54\cdot 10^{10}}{E_{inj}}\right]} \quad (2\text{-}1)$$

where $E_{inj}$ is the field strength at the oxide surface through which the tunneling will occur. A 6.4 MV/cm injection field results in an injection current density of 2.74 μA/m$^2$. This produces extremely low tunneling currents with device feature sizes at the sub-micron level.

Hot electron injection is the more limited of the two programming options. This technique involves placing a $V_{DS}$ bias across the device as well as a $V_{GS}$ bias. These conditions allow an electron traveling through the channel to tunnel through the gate oxide near the drain. This method has the advantage of needing lower voltages to create tunneling, but it has the drawbacks of only providing tunneling ability onto the floating gate, having an unpredictable tunneling rate for which there is no closed form solution [4], as well as being far more destructive. In addition, hot-electron tunneling requires a channel current from which it can draw its tunneling electrons. Therefore the current requirement for such hot-electron programming is much higher than that of Fowler-Nordheim tunneling.

Although the Ohsaki FGD design originally utilized both Fowler-Nordheim tunneling and hot electron injection as programming methods (in 0.8μm bulk CMOS), experimental tests using devices manufactured in a 0.5μm bulk CMOS process produced

no noticeable hot electron effects. This is most likely due to the inclusion of lightly doped drain regions in modern manufacturing to help combat short-channel effects. This preventative measure will only become more prevalent as device feature sizes continue to shrink. Therefore Fowler-Nordheim tunneling is the chief programming option in modern FGD manufacturing processes. The configuration for Fowler-Nordheim programming is shown in Figure 2.3. A programming voltage pulse ($V_p$) is applied at the control gate and divided over the gate capacitances to create an electric field that allows electrons to tunnel from the *n*MOS section of the FGD structure, through the gate oxide, and become trapped on the floating gate. This additional charge raises the threshold of the *n*MOSFET device. Connecting the structure in the manner shown in Figure 2.4 allows the threshold of the FGD's *n*MOSFET to be lowered by creating a field that causes electrons trapped on the floating gate to tunnel back through the *n*MOS gate oxide. In both cases care must be taken to avoid reverse breakdown conditions. For the programming operation, the junction to watch is the *n*-well to *p*-substrate junction; for the erasing operation the junction to be concerned about is the *n*+ to *p*-substrate junction of the *n*MOS side of the FGD.

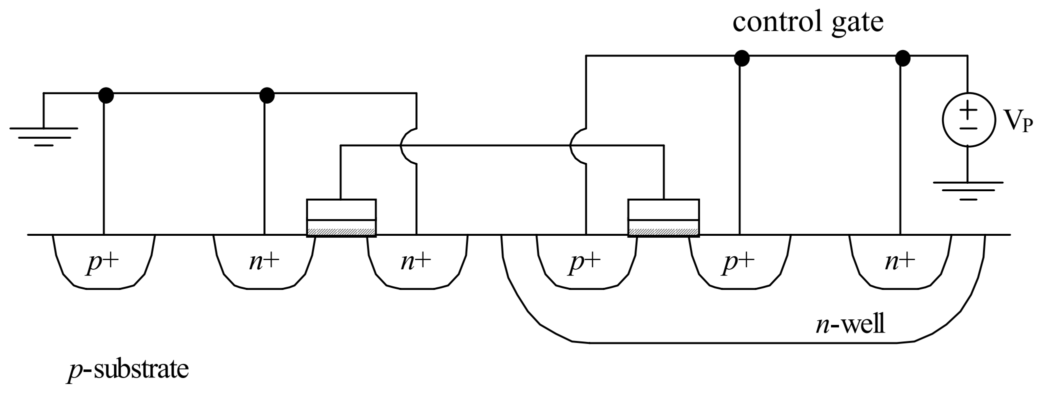


Figure 2.3. Programming Configuration for Single-Poly FGD [2]

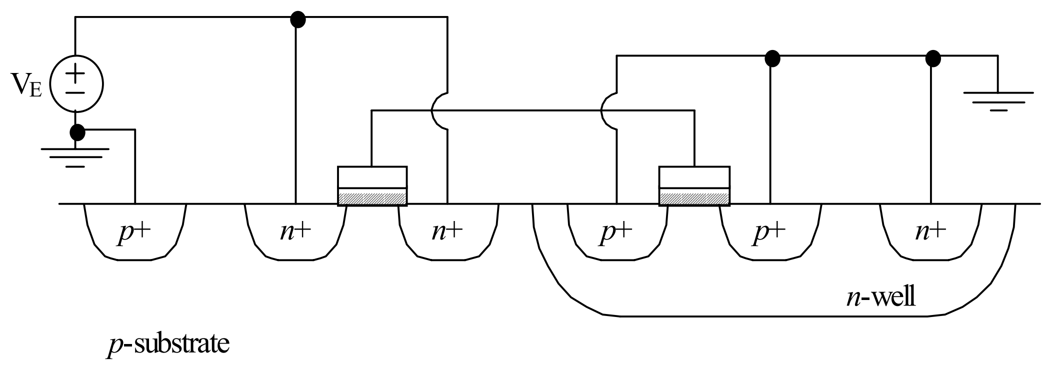


Figure 2.4. Erasing Configuration for Single-Poly FGD [2]

In both the programming and deprogramming case, it is assumed that tunneling occurs through both *n*MOS and *p*MOS gate oxides. However, the density of electrons in the *n*+ source/drain diffusions and *n*-type inversion layer allow more tunneling to occur through the *n*MOS gate oxide than through the *p*MOS gate oxide.

The extremely low current levels required for this type of programming technique makes on chip threshold adjustment a very real possibility through the use of devices capable of producing the required relatively high programming and erasing voltages. A very likely candidate for the key component of such on chip arrangements is any of the variety of available charge pumps, such as the "voltage doubler" put forth in [7].

## 2.5 Experimental Programming/Deprogramming Results

Nine different FGDs manufactured in a 1.2µm AMI bulk CMOS process were tested. Four of these devices were designed with larger, square gates on the *n*MOS side of the device in the hopes of utilizing increased electromagnetic fields at the corners of the gates to aid in producing greater tunneling effects. These square gates, however, (compared in Figure 2.5) showed no performance improvement over the straight gates.

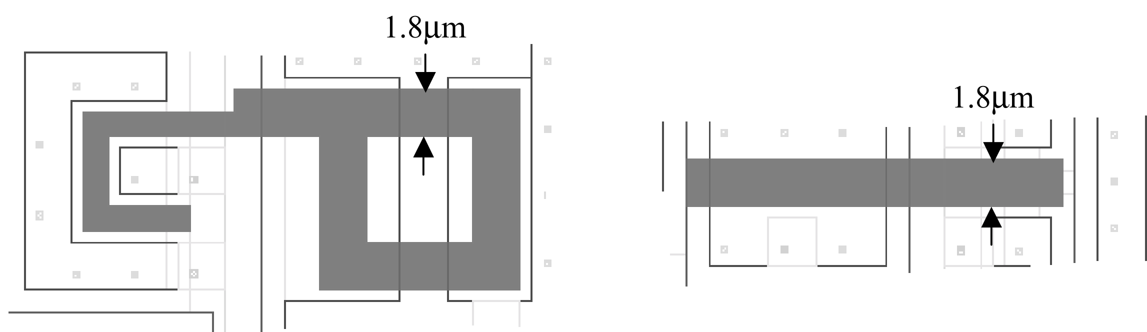


Figure 2.5. Square Gate and Straight Gate Comparison

Table 2.1 shows the widths and lengths of the five straight gate FGDs. There are two separate pairs of identical gates listed. FGDs 2 and 3 share the same *n*-well, but FGDs 4 and 7 reside in separate *n*-wells.

Table 2.1

DIMENSIONS OF STRAIGHT GATE FGDS

| | *P*MOS | | *N*MOS | |
|---|---|---|---|---|
| Device Number | Width (μm) | Length (μm) | Width (μm) | Length (μm) |
| 2 | 9 | 1.2 | 1.8 | 1.2 |
| 3 | 9 | 1.2 | 1.8 | 1.2 |
| 4 | 9 | 2.4 | 1.8 | 2.4 |
| 7 | 9 | 2.4 | 1.8 | 2.4 |
| 8 | 3.6 | 1.2 | 1.8 | 1.2 |

Threshold voltages were extracted from the test devices through the use of an HP 4145 by placing a small (200mV) voltage across the drain and source terminals of the device while sweeping the gate-to-source voltage. Extracting the zero-intercept of an $(I_{DS})^{0.5}$ curve, as described in [8] provided the threshold voltage.

Figures 2.6 and 2.7 illustrate programming and deprogramming performance of the straight gate FGDs. Experimental programming was performed to establish its

feasibility, not to establish its absolute range. Erasing was performed on the devices to lower the thresholds from the abnormally high levels they arrived at. Presumably these high initial thresholds were due to charge trapped during the plasma etching of the devices. For programming the FGDs, square wave pulses were taken from an HP 33120A signal generator and amplified by an Intersil HA-2640 operational amplifier to provide a 12V magnitude, 50kHz signal of 50% duty cycle. This configuration provided 10µs pulses of programming voltage separated by 10µs downtimes. This signal was monitored by use of an HP 54616C oscilloscope. For deprogramming, the pulses were of 15V magnitude with a 10kHz frequency. This resulted in 15V pulses of 50µs lengths occurring with 50µs spacing between them.

A higher magnitude, longer duration pulse was required for erasure due to the signal being capacitively divided across the *n*MOS and *p*MOS sections of the FGD. The relative sizing of the two halves of the devices aided in programming but provided a hindrance during erasure. As Figure 2.6 and Table 2.1 illustrate, decreasing the *p*MOS gate capacitance while maintaining identical sizing on the *n*MOS side of the FGD greatly reduces the effectiveness of a given programming pulse. Presumably a similar relationship between the *n*MOS sizing with fixed *p*MOS dimensions and deprogramming time also exists.

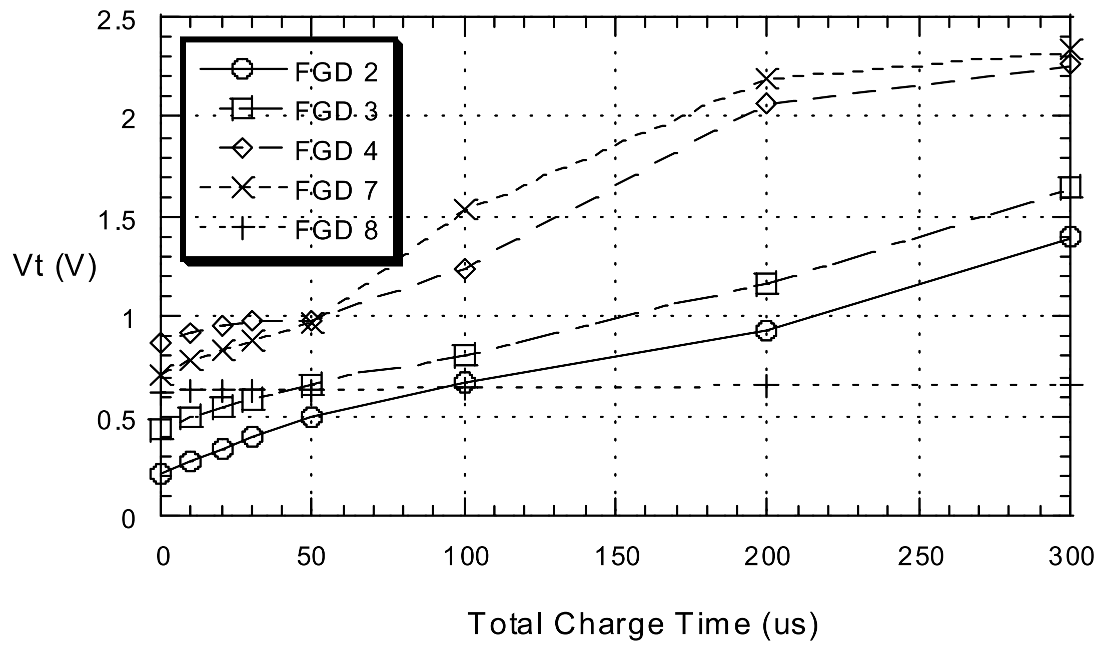


Figure 2.6. FGD Programming Test Results

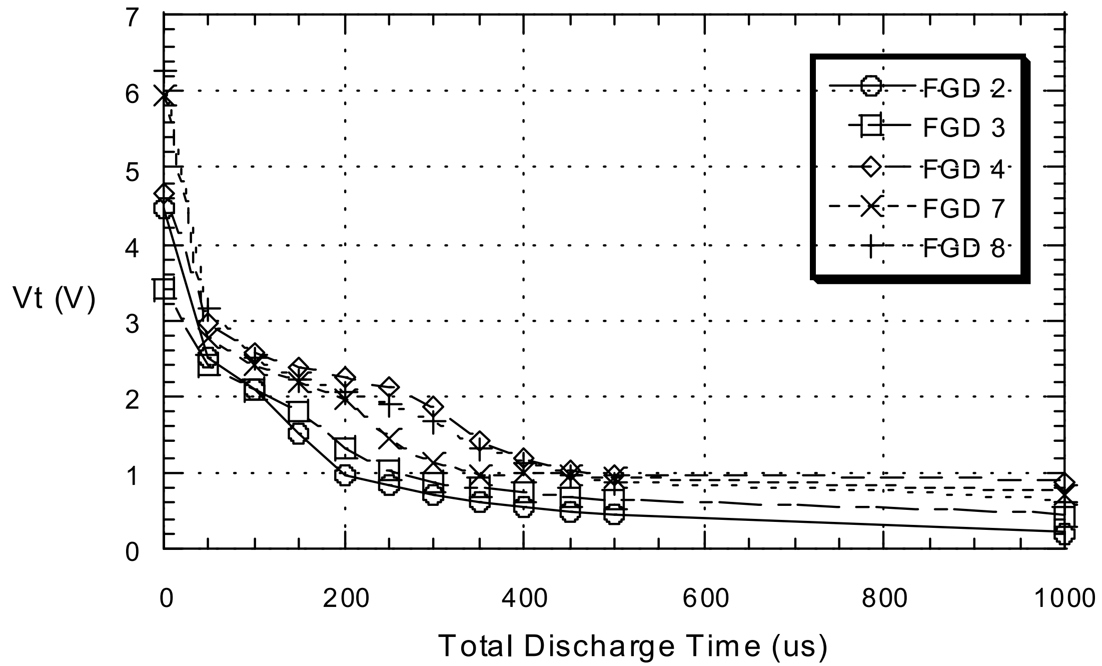


Figure 2.7. FGD Deprogramming Test Results

## 2.6 Conclusion

The FGD structure proved both programmable and erasable with reasonable adjustment voltages using only Fowler-Nordheim tunneling. This will allow these devices to provide flexible operation, such as in the two circuits proposed in this thesis.

# CHAPTER III

# TUNEABLE SIMPLE CURRENT MIRROR

## 3.1 Simple Current Mirror

One of the most fundamental building blocks of MOSFET analog/mixed signal systems is the simple current mirror. This basic circuit, shown below in Figure 3.1, functions by forcing an identical $V_{GS}$ across both M1 and M2.

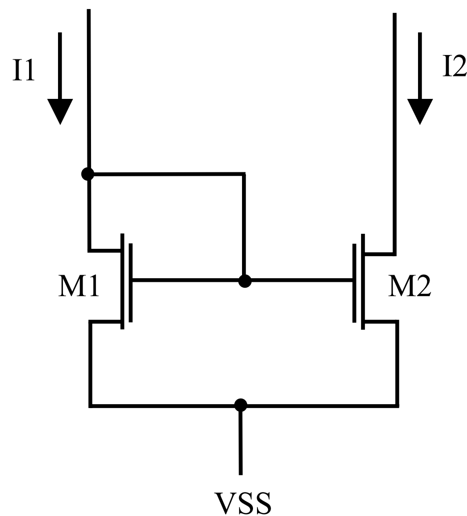


Figure 3.1. Simple Current Mirror.

As long as both M1 and M2 are in saturation, this configuration yields the current relationship given by [9]

$$I2 = I1 \cdot \frac{\beta_2}{\beta_1} \qquad (3\text{-}1)$$

This relationship enables a reference current (I1) to be copied by simply adding a single transistor, M2. Unfortunately, copying a current like this will inevitably result in small differences in I1 and I2 due to process variations, channel length or mobility modulation, uneven chip heating, or any of a variety of other factors. The closer that $\beta 1$ matches $\beta 2$, the closer the output current (I2) will resemble the input current (I1). As these mirrored currents are often used to bias circuit components to specified operating points, variations in these currents can be quite problematic if they occur in sensitive components such as a differential pair within an operational amplifier's input stage. Thus, keeping these devices and the currents they provide as well matched as possible is of utmost importance in analog design.

### 3.2 Tunable Simple Current Mirror

The idea of an adjustable current mirror for such applications appeals to designers for several reasons. First, it adds the obvious advantage of post-fabrication adjustments to help matching. Such a device would also allow for corrections of minor design flaws to be made that would otherwise cause problems (such as an incorrect biasing level). Also, the flexibility of these devices may ultimately allow "flexible" analog standard cells to be developed for a mixed-signal library. This tunability can save design time

(and therefore money). A final advantage is that if a design specification changes, having an adjustable device allows much greater design flexibility and avoids the need for redesign and subsequent fabrication cost.

To create such a tunable simple current mirror, FGDs are used to replace the MOSFETs from Figure 3.1 to provide the circuit shown in Figure 3.2. Both transistors are replaced with FGDs to aid in geometric matching as well as gate-source voltage matching [2]. This configuration allows the reference section of the mirror to be fine tuned by making adjustments to the threshold voltage of M1, and it allows mirrored current to be adjusted by altering the threshold FGD M2. Note that by replicating FGD M2, additional output legs (mirrored currents) can be provided. Such multi-leg adjustable currents allow selective tuning of more sensitive sections of a circuit while freeing up circuit programming and deprogramming time from less sensitive legs.

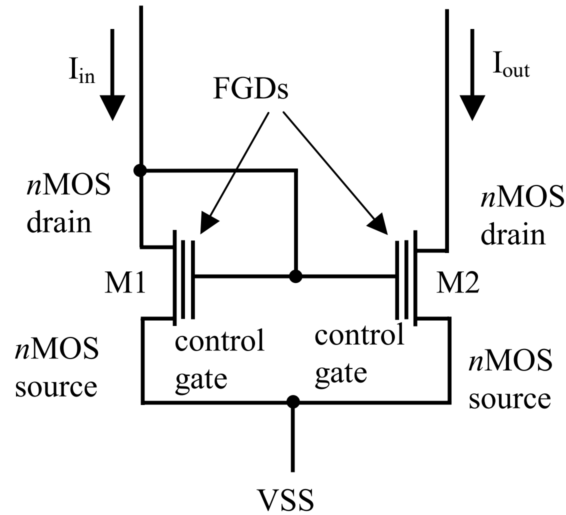


Figure 3.2. Tunable Simple Current Mirror

## 3.3 Experimental Results

A test mirror was constructed by connecting two identically sized devices from two separate die in the manner shown in Figure 3.2. These test devices were fabricated in a Hewlett Packard 0.5μm bulk CMOS process. Each leg was constructed from an *n*MOS FGD device whose sizing measurements were as follows: the W/L measurements of the *n*MOS side of the FGD were 1.8μm/1.2μm and the W/L measurements of the *p*MOS side of the FGD were 9μm/1.2μm. Figure 3.3 shows the performance of the mirror initially. This current data was taken with an HP 4145 configured to hold each leg to a constant voltage (250mV) while sweeping the input current. After each sweep the FGD with the higher threshold voltage was erased, as described in section 2.5. The choice of erasure of

the high threshold instead of programming the lower threshold device threshold device was an arbitrary test setup decision. The goal of the adjusting process was to achieve a high degree of accurate matching at a 30□A input current. Figures 3.4 and 3.5 show curves taken at the midpoint and final point in the adjustment process.

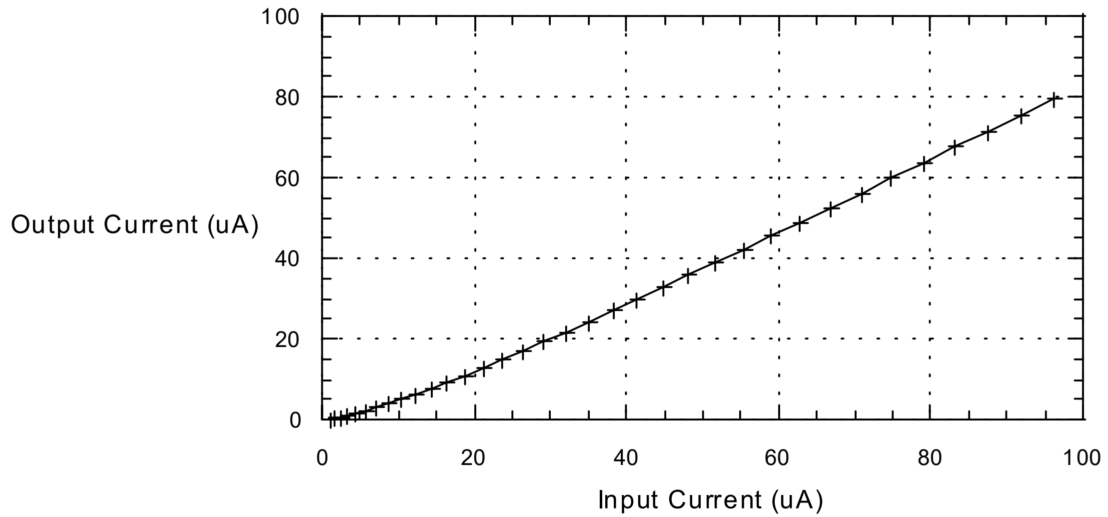


Figure 3.3. Initial Current Sweep of Mirror

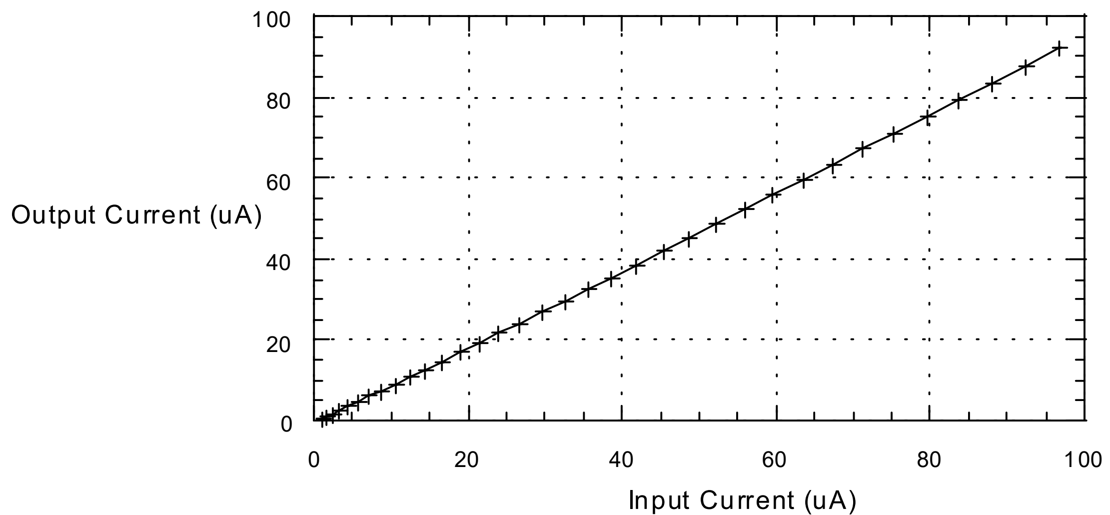


Figure 3.4. Current Sweep of Mirror After 150μs Erasure Adjustment

This level of adjustment showed significant improvement in matching compared to the initial sweep. Additional adjustment was applied to fine tune the matching (i.e. smaller number of erasure pulses were applied between measurements) resulting in the curve shown in Figure 3.5.

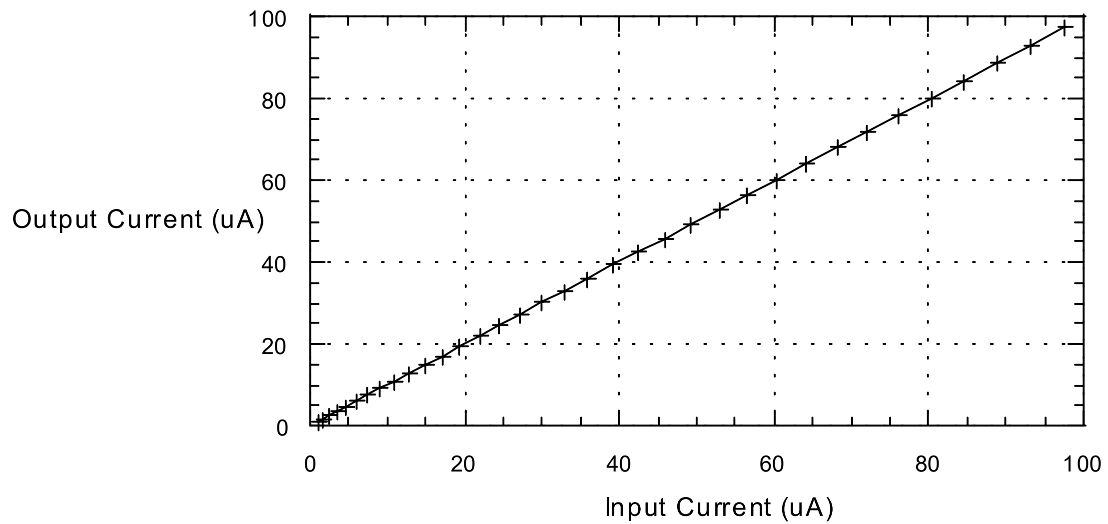


Figure 3.5. Current Sweep of Mirror After 242µs Erasure Adjustment

It is easy to see there is a very high degree of accuracy at the end of the adjustment process. Figure 3.6 illustrates the mismatch between the input and output currents at the targeted current level (30µA) throughout the adjustment process.

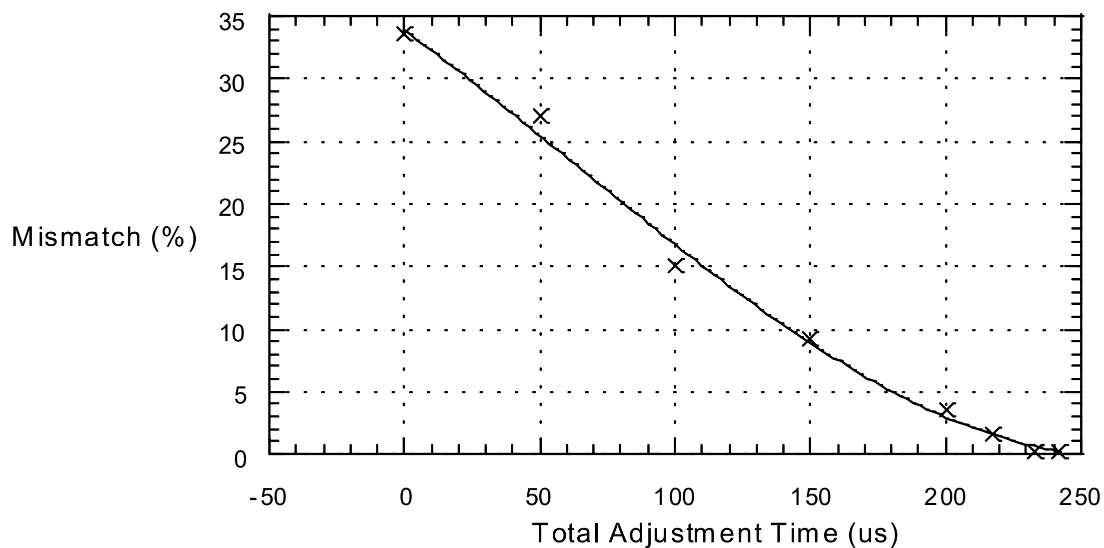


Figure 3.6. Current Mismatch at 30 $\mu$A Over the Adjustment Period

This matching adjustment was performed on three separate mirrors resulting in worst case matching from three separate mirrors on separate die of only 0.04% at 30 $\mu$A [2]. Matching at this level with a conventionally constructed current mirror would only be obtainable by using much more massive transistors for improving transistor matching [2]. Thus, this tunable current mirror provides high precision current matching with very small silicon area.

CHAPTER IV

# TUNEABLE BETA-MULTIPLIER

## 4.1 Beta-multiplier Current Reference

A second crucial component for any type of analog or mixed signal design is the reference circuit. This component generates the reference level, either a voltage or a current, upon which everything in the system is based. For example, a reference current can be mirrored throughout a design to create the correct bias for individual stages.

The tunable reference put forth in this thesis is based on the conventional beta-multiplier topology described in [9]. The conventional circuit is shown in Figure 4.1. This design produces a reference current, $I$, described by

$$I = \frac{2}{R^2 \beta_1} \cdot \left(1 - \sqrt{\frac{1}{K}}\right)^2 \qquad (4\text{-}1)$$

[9]. In this relationship, $K$ is the term relating $\beta_1$ to $\beta_2$ as given below.

$$K = \frac{\beta_2}{\beta_1} = \frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}} \qquad (4\text{-}2)$$

These relationships show that in order to set *I* at a desired level, both *R* and *K* must be chosen. Typically a *K* value of 4 is selected so that both M1 and M2 can easily remain in identical operation modes (such as strong inversion saturation) to maintain optimal matching. The resistor, *R*, must be designed (in layout) to generate as close to the ideal calculated resistance as possible. This can be problematic when process variations can induce 10% to 30% changes in passive resistor values in a standard CMOS process. It becomes even more difficult to achieve an ideal current reference output when other variations such as temperature are included.

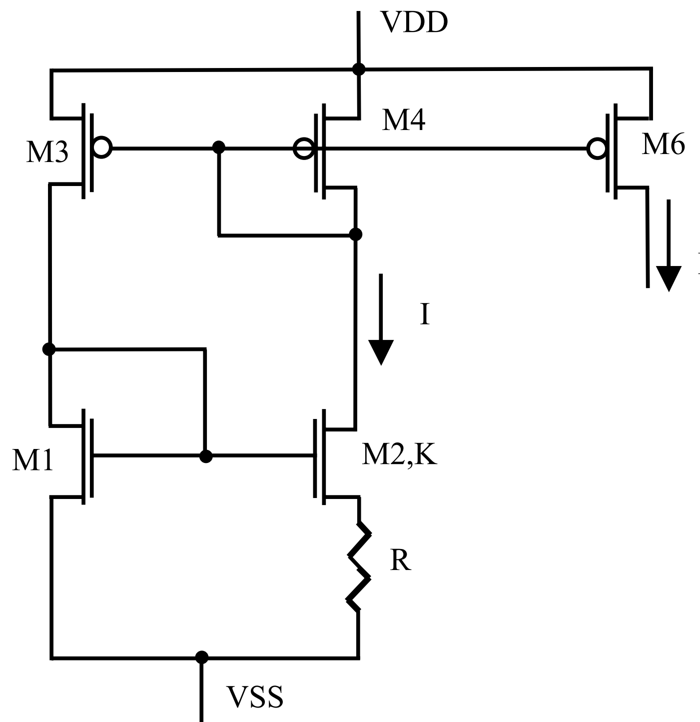


Figure 4.1. Conventional Beta Multiplier Reference Circuit [9]

## 4.2 Tunable Beta-multiplier Current Reference

A tunable current source helps eliminate these problems. Simply replacing the standard beta-multiplier's resistor with a FGD that has been programmed to operate as a depletion-mode (negative $V_T$) MOSFET creates a tunable current reference whose programmable resistor should also provide temperature compensation in some applications. This unique circuit is shown below in Figure 4.2.



Figure 4.2. Tunable Beta-multiplier Current Reference

By insuring that the FGD is operated in triode (linear) mode and connecting it as shown above, the FGD functions as a resistor whose value is expressed in Equation (4-3) where $V_T$ is the *n*MOS threshold of the FGD and $\beta_R$ is the transconductance parameter of the *n*MOS section of the FGD (as defined in Equation (4-4)).

$$R \approx -\frac{1}{\beta_R \cdot V_T} \tag{4-3}$$

$$\beta_R = \mu_n C_{OX} \left( \frac{W}{L} \right)_{nMOS,FGD} \tag{4-4}$$

### 4.3 Experimental Results

A selection of the straight gate FGDs used in section 3 were erased until they became depletion devices. Typical results from these FGDs after erasing them until they operated as depletion devices (and resistors) are shown in Figure 4.3. In this figure *n*MOS width to length ratios of 1.5 to 1 and 1 to 1.5 are shown. The HP FGDs used in this experiment were arranged on the chip exactly as the AMI FGDs, as discussed in section 2.5.

As clearly shown in Figure 4.4, a great range of resistance is possible from the same FGD. This range allows the output current of the tunable current reference to be greatly altered by adjusting the *R* value in Equation (4-1) as long as care is taken to keep the device operating in the linear region. Maintaining the FGD in linear operation is achieved by insuring that the condition

$$(V_{DS})_R \bullet \bullet (V_{GS} \bullet \bullet V_T)_R \qquad (4\text{-}5)$$

is maintained.

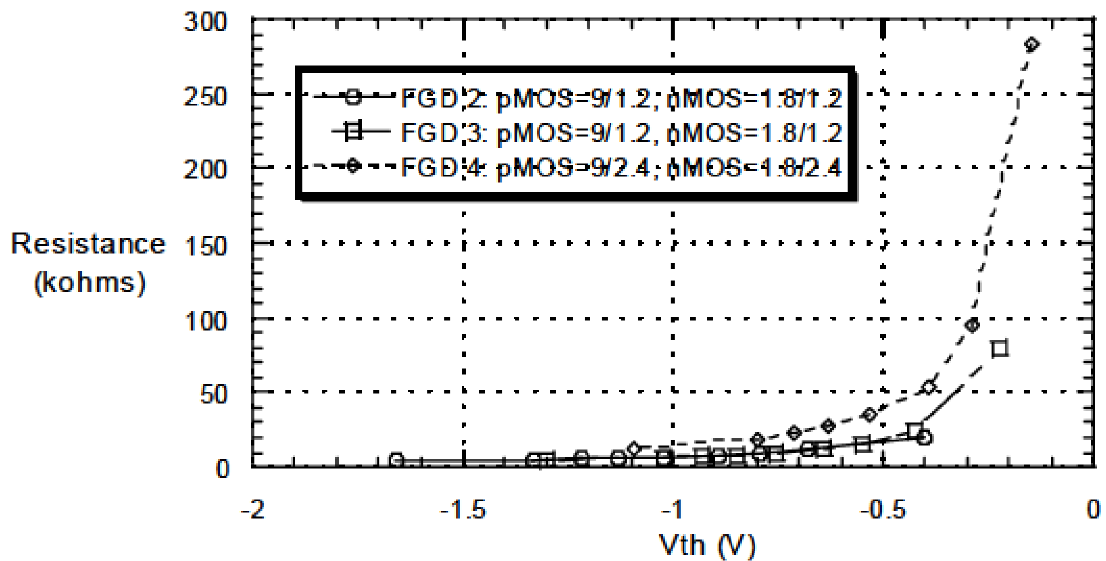


Figure 4.3. Resistance Values of FGD in a 0.5µm HP Process

Figures 4.4 and 4.5 illustrate the consistency of these results by comparing test results from four separate die on identical devices whose *n*MOS width to length ratio is 1.5 to 1 for Figure 4.5 and whose *n*MOS width to length ratio is 1 to 1.5 for Figure 4.6.

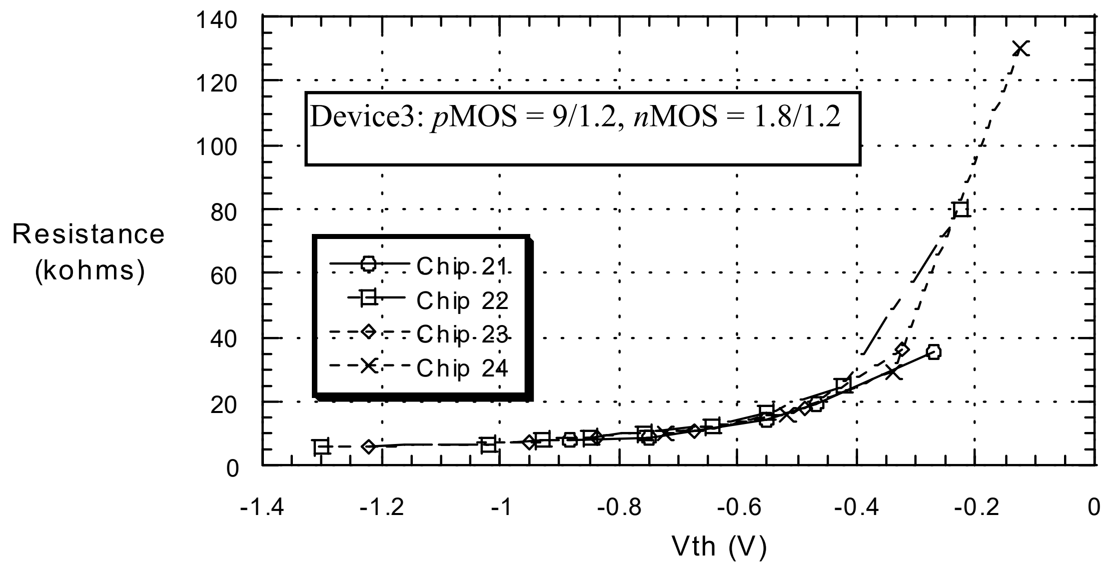


Figure 4.4. FGD programmable resistance comparison between multiple die for *n*MOS W/L of 1.5/1

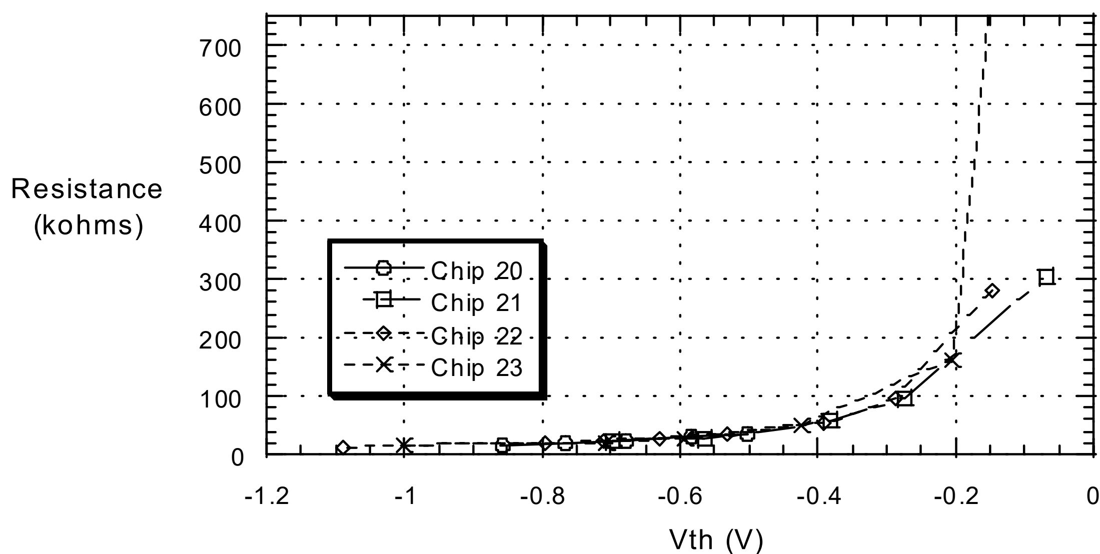


Figure 4.5. FGD programmable resistance comparison between multiple die for *n*MOS W/L of 1/1.5

Figures 4.4 and 4.5 clearly illustrate that a given FGD design maintains very similar performance from chip to chip. This consistency is quite an advantage for the FGD over most standard CMOS resistors. Another advantage of the FGD over a standard resistor for many applications is the reduction in chip area. Despite having to use the area of both an *n*MOSFET and a *p*MOSFET, the FGD can achieve resistances on the order of k□ in a tiny fraction of the layout area required by an on-chip poly or diffusion resistor. This is especially true if the process does not have the option of non-

silicided polysilicon. In a digital process, normally a nonsilicide (or silicide "blanking") mask option is not provided.

Examining this reference for its theoretical temperature behavior yields interesting results. Inserting Equation (4-3) into (4-1) results in Equation (4-6) for $I_{out}$.

$$I_{out} = \frac{2}{\left(\frac{1}{(\beta \cdot V_T)_{nMOS,FGD}}\right)^2 \beta_1} \cdot \left(1 - \sqrt{\frac{1}{K}}\right)^2 \qquad (4\text{-}6)$$

Choosing a typical value for $K$ (4), and including (4-4), allows (4-6) to be simplified into

$$I_{out} = \frac{\left(\frac{W}{L}\right)^2_{nMOS,FGD}}{\left(\frac{W}{L}\right)_1} \cdot \frac{\mu_n \cdot C_{ox}}{2} \cdot (V_T)^2_{nMOS,FGD}. \qquad (4\text{-}7)$$

Grouping terms leads to

$$I_{out} = A \cdot \mu_n \cdot (V_T)^2_{nMOS,FGD}, \qquad (4\text{-}8)$$

where

$$A = \frac{\left(\frac{W}{L}\right)^2_{nMOS,FGD}}{\left(\frac{W}{L}\right)_1} \cdot \frac{C_{OX}}{2} \tag{4-9}$$

Taking the derivative of $I_{out}$ with respect to temperature generates the relationship

$$\frac{\partial I_{out}}{dT} = A\left[\left(\frac{\partial}{dt}\mu_n\right)\cdot\left(V_T\right)^2_{nMOS,FGD} + \mu_n \cdot \frac{\partial}{dt}\left(V_T^2\right)_{nMOS,FGD}\right] \tag{4-10}$$

Inserting (4-10) into the temperature coefficient (*TC*) relationship shown in Equation (4-11) gives the *TC* of the tunable reference (Equation (4-11)).

$$TC_{I_{OUT}} = \frac{1}{I_{out}} \cdot \frac{\partial I_{out}}{dT} \tag{4-11}$$

$$TC_{I_{OUT}} = \frac{1}{\mu_n} \cdot \frac{\partial \mu_n}{dt} + 2 \cdot \frac{1}{\left(V_T\right)_{nMOS,FGD}} \cdot \frac{\partial \left(V_T\right)_{nMOS,FGD}}{dT} \tag{4-12}$$

Substituting typical standard CMOS values for mobility from [9] and $V_T$ variation extracted from simulation of a typical 0.5μm HP process results in Equation (4-13). This equation shows the theoretical result of adjusting the FGD threshold with respect to the circuit's temperature coefficient.

$$TC_{I_{OUT}} \cong -\frac{1.5}{T} \cdot \frac{2}{(V_T)_{nMOS,FGD}} \cdot \left(-0.365\frac{mV}{^0C}\right) \quad (4\text{-}13)$$

HSPICE was used to simulate this proposed tunable beta-multiplier current reference using HP 0.5µm models from MOSIS with the FGD resistor represented as shown in Figure 2.2. This simulated reference was designed to produce a 20µA current at 27° C. The simulation produced the "simulated" TCs shown in Figure 4.7. At each new value of threshold voltage, the W/L ratio of the *n*MOS section of the FGD was adjusted to produce a current of 20µA ±5%. Figure 4.7 also shows values of TC, as calculated with Equation (4-13), over an identical threshold voltage range. This set of data is the one labeled "first theory."

The near constant gap across most of the curve in Figure 4.7 seems to indicate different carrier mobility between the simulated circuit and the calculated values. This disparity would affect the first term in Equation (4-13) producing such a linear offset (approximately 2200ppm). Adjusting the numerator of carrier mobility term from –1.5 to –2.15 produced the data line labeled "adjusted theory." The "bump" in the simulated values between thresholds of –0.3V and –0.7V is most likely due to the loose constraint (±5%) the current was required to meet during simulation. The increasing disparity between simulation and theoretical calculation as Vth becomes less negative is most

likely the result of terms becoming more dominant that are neglected in the theoretical equation.

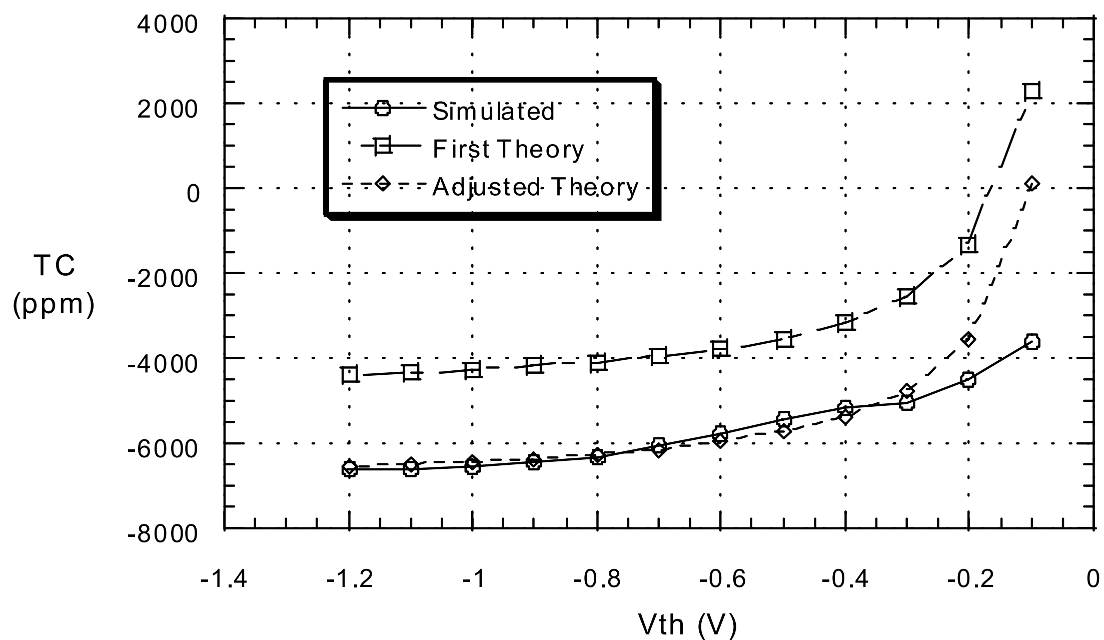


Figure 4.6. Comparison of TC Values for Tunable Reference Circuit

Utilizing these equations results in a straightforward design technique for the tunable reference. First, a $V_T$ is chosen for the FGD to provide the desired *TC* at a given temperature. Then a value is selected for *A* (Equation (4-9)) to provide the desired $I_{out}$.

One complication for using the tunable reference is designing the tuning ability into the reference. Switches must be included to isolate the FGD from the rest of the

circuit (between the source of M2 and the drain of the FGD) and to switch the control gate connection from ground to the programming pulse. Similar connection rerouting is necessary to provide the ability to erase a programmed FGD in this circuit. An example circuit including the needed switches is shown below in Figures 4.7 and 4.8.

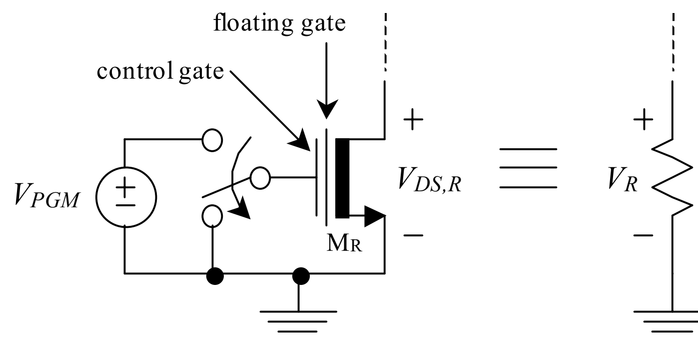


Figure 4.7. Partial Switching Diagram for FGD used as a Resistor

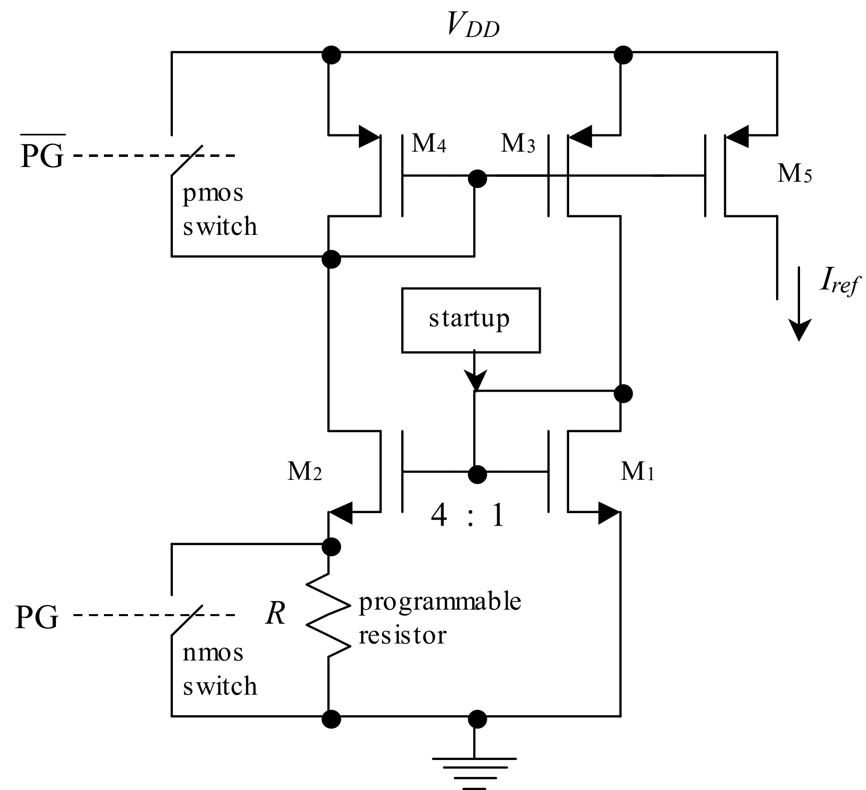


Figure 4.8. Switching Diagram for Programmable Reference

# CHAPTER V

# CONCLUSION

Experimental results confirm the operation of the FGD. Both programming and deprogramming operations proved successful, obtaining a wide range of threshold voltages. The FGDs were successfully tested operating under a variety of conditions. In all cases the FGDs functioned as conventional *n*MOSFETs under identical conditions.

The tunable simple current mirror performed very well. With a measured matching level of better than 0.04% in the targeted current range, it demonstrated that with the replacement of a current mirror's MOSFETs with FGDs provides a very high precision current mirror in a comparatively small area.

The programmable current reference provides interesting theoretical data. Although the circuit has not been fabricated, the experimental data of the FGD functioning as a resistor and the theoretical temperature performance both provided encouraging results.

There are several possible areas of future work with these designs. The first potential future project is the creation and verification of a *p*MOS version of the FGD. Another variant of the FGD of interest would be one with twin control gates. Also, implementing the current reference on chip for experimentation should prove helpful in

both verifying its predicted functionality and allowing examination of its temperature performance. This would of course require designing the necessary on-chip programming network.

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